REMARKS

Claims 1-30 were pending in the present application. Claims 8 and 9 have been amended. Accordingly, claims 1-30 remain pending in the application.

Claims 8, 9, 22, and 29 stand rejected under 35 U.S.C §112, 2nd paragraph, as being indefinite. Applicant respectfully traverses a portion of this rejection. More particularly, Applicant has amended claims 8 and 9 to overcome the rejection. However, Applicant submits claims 22 and 29 have proper antecedent basis. Claims 22 and 29 depend from claim 21. As shown above, claim 21 recites "an additional node" in the preamble. Thus, there is proper antecedent basis for the phrase "the additional node" as recited in claims 22 and 29.

Claims 1-30 stand rejected under 35 U.S.C. §102(b) as being anticipated by Liencres et al. (U.S. Patent No. 5,434,993) (hereinafter " Liencres"). Applicant respectfully traverses this rejection.

Applicant's claim 1 recites

"A node for use in a multi-node system, the node comprising:

a plurality of active devices;

an interface to an inter-node network coupling nodes in the multi-node system; and

an address network configured to convey address packets between the interface and the plurality of active devices;

wherein an active device of the plurality of active devices is configured to send an address packet on the address network to initiate a transaction to gain an access right to a coherency unit;

wherein in response to the address packet, the interface is configured to send data corresponding to the coherency unit to the active device **if no other active device in the node has an ownership responsibility** for the coherency

unit **and** the coherency unit is in a modified global access state in the node." (Emphasis added)

The Examiner asserts Liencres teaches each and every limitation recited in Applicant's claim 1. More particularly, the Examiner asserts Liencres teaches in FIG. 3a, the plurality of active devices as elements 21, 31, and 32, the internode network as also being element 31, an address network coupling the active device and the interface as also being element 33. Applicant respectfully disagrees with the Examiner's characterization of Liencres and the application of Liencres to Applicant's claims.

Specifically, as illustrated in Fig.3a and 3b of Liencres, element 31 is the bus cache controller and not an active device. Both element 32 and 21 can't be active devices since element 32 is a processor module that includes element 21(the processor). Element 33 cannot be the address network as recited in Applicant's claim 1 because it only couples the bus controller 31 to the processor cache controller 35, or the processor module to additional bus cache controllers as shown in Fig. 3b. It does not couple the active device (processor), the interface (element 31), and the memory 23 as recited in claim 1. Thus, there are not multiple active devices in the node 20 of Liencres, because Liencres is only teaching a multiprocessor system in which each node only includes a single processor 21.

Furthermore, Applicant asserts Liencres actually teaches at col. 6, lines 50-60

> "The cache bus 33 can be used by the processor module 32 to support multiple bus cache controllers coupled to separate memory buses. Referring to FIG. 3b, an alternate embodiment of the present invention with two memory buses is illustrated. In the embodiment of FIG. 3b, a processor module 32 is coupled to a cache bus 33 which has two separate bus cache controllers 30 and 31. Each bus cache controller 30 and 31 controls bus transactions on a separate memory bus. The separate memory buses each have their own associated main memory units 22 and 24."

From the foregoing, Applicant asserts Liencres is merely teaching that more than one bus controller 31 may be coupled to a given processor module 32 which facilitates processor module 32 communicating with more than one memory via more than one

memory bus as shown in Fig. 3b of Liencres. Applicant submits Liencres does not teach or disclose "in response to the address packet, the interface is configured to send data corresponding to the coherency unit to the active device **if no other active device in the node has an ownership responsibility** for the coherency unit **and** the coherency unit is in a modified global access state in the node" based on this passage.

Accordingly, Applicant submits claim 1, along with its dependent claims, patentably distinguishes over Liencres for the reasons given above.

Applicant's claim 11 recites features that are similar to the features recited in claim 1. Thus Applicant submits claim 11, along with its dependent claims, patentably distinguishes over Liencres for at least the reasons given above.

Claim 21 recites method comprising in pertinent part

> "in response to the address packet, an interface to the inter-node network included in the node sending data corresponding to the coherency unit to the active device **if** no other active device in the node has an ownership responsibility for the coherency unit **and** the coherency unit is in a modified global access state in the node." (Emphasis added)

As described above, these features are not taught in Liencres. Accordingly, Applicant submits claim 21, along with its dependent claims, patentably distinguishes over Liencres for the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-99001/SJC.

Respectfully submitted,

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